

AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method comprising:

receiving a plurality of ~~consecutive requests to access a memory, each of the~~ plurality of ~~memory access~~ requests specifying one address in a range of multiple, sequential addresses;

determining if an address corresponding with one of the plurality of requests is within the range of multiple addresses ~~decoding each of the multiple addresses to produce a decoded address; and~~

causing a memory to be accessed ~~accessing the memory whenever an~~ address corresponding with a request is within the range of multiple addresses, ~~if the decoded address is a first address, wherein the memory being is identified by and accessible only through a single the first address, whereby the memory is accessed using any one of the addresses in the range of multiple addresses.~~

2. (currently amended) The method of claim 1, further comprising ~~requesting a burst mode access to the memory, the burst mode access request defining the multiple addresses, and, in response to the burst mode access request, sending the plurality of consecutive requests in a sequence, wherein the address corresponding with each successive request in the sequence is a successive address in the range of multiple addresses, to access the memory, each of the plurality of requests specifying one of the multiple memory addresses.~~

3. (currently amended) The method of claim 17, wherein ~~accessing the memory access if the decoded address is the first address~~ includes reading from the memory.

4. (currently amended) The method of claim 17, wherein ~~accessing the memory access if the decoded address is the first address~~ includes writing to the memory.

5. (currently amended) An apparatus comprising:

a memory device identified by and accessible only through a single ~~at a first~~ address; and

at least one unit decoder to receive a plurality of requests, each of the plurality of requests specifying one address in a range of multiple addresses from a bus, to determine produce a decoded address if an address corresponding with one of the plurality of requests a received address is within the range one of a particular plurality of multiple addresses, and to cause the memory device to be accessed whenever an address corresponding with a request is within the range of multiple addresses, whereby the memory is accessed using any one of the addresses in the range of multiple addresses. if the decoded address is the first address.

6. (currently amended) The apparatus of claim 5, wherein the particular plurality of requestsaddresses are sequential and the address corresponding with each successive request in the sequence is a successive address in the range of multiple addresses.

7. (currently amended) The apparatus of claim 5, wherein the memory access caused by the at least one decoder, if the decoded address is the first address, is a read access.

8. (currently amended) The apparatus of claim 5, wherein the memory access caused by the at least one decoder, if the decoded address is the first address, is a write access.

9. (currently amended) A medium readable by a machine embodying a program of instructions executable by the machine to perform a method, the method comprising the steps of:

receiving a plurality of consecutive requests to access a memory, each of the plurality of ~~memory access~~ requests specifying one address in a range of multiple addresses;

determining if an address corresponding with one of the plurality of requests is within the range of multiple addresses ~~decoding each of the multiple addresses to produce a decoded address;~~ and

causing a accessing the memory if the decoded address to be accessed whenever an address corresponding with a request is within the range of multiple addresses, is a first address, wherein the memory is being identified by and

accessible only through a single ~~the first address,~~ whereby the memory is accessed using any one of the addresses in the range of multiple addresses.

10. (currently amended) The medium of claim 9, wherein the method further comprises ~~requesting a burst mode access to the memory, the burst mode access request defining the multiple addresses, and, in response to the burst mode access request, sequentially sending the plurality of consecutive requests in a sequence, wherein the address corresponding with each successive request in the sequence is a successive address in the range of multiple addresses, to access the memory, each of the plurality of requests specifying one of the multiple memory addresses.~~

11. (currently amended) The medium of claim 9, wherein the ~~accessing the memory~~ access ~~if the decoded address is the first address~~ includes reading from the memory.

12. (currently amended) The medium of claim 9, wherein the ~~accessing the memory~~ access ~~if the decoded address is the first address~~ includes writing to the memory.

13. (currently amended) A system for burst mode data transfers, comprising:

a bus;

a processor, coupled with the bus, ~~to execute an instruction to place a plurality of requests a particular plurality of addresses on the bus, each of the plurality of requests specifying one address in a range of multiple addresses;~~

a memory, coupled with the bus, the memory being identified by and accessible only through a single ~~at a first address;~~ and

at least one unit ~~decoder~~, coupled with the bus and with the memory, to receive the plurality of requests ~~addresses~~ from the bus, to determine if produce a decoded an address if a received address corresponding with ~~is~~ one of the particular plurality of requests is within the range of multiple addresses ~~addresses~~, and to cause the memory to be accessed whenever an address corresponding with a request is within the range of multiple addresses, whereby the memory is accessed using any one of the addresses in the range of multiple addresses, if the decoded address is the first address,

14. (previously presented) The system of claim 13, wherein the memory is a first-in-first-out memory.

15. (currently amended) The system of claim 14, wherein ~~the processor, responsive to the instruction to place a particular plurality of addresses on the bus, sends a plurality of consecutive requests on the bus to~~ the memory access is a read access from the memory, each of the plurality of requests specifying one of the particular plurality of addresses.

16. (currently amended) The system of claim 14, wherein ~~the processor, responsive to the instruction to place a particular plurality of addresses on the bus, sends a plurality of consecutive requests on the bus to~~ the memory access is a write access to the memory, each of the plurality of requests specifying one of the particular plurality of addresses.

17. (currently amended) The method of claim 12, wherein the memory is a first-in-first-out memory.

18. (currently amended) The apparatus of claim 5, wherein the memory device ~~accessible at the first address is~~ a first-in-first-out memory.

19. (currently amended) The apparatus of claim 5, wherein ~~the at least one decoder receives from the bus a plurality of consecutive requests to access the memory, each of the consecutive requests specifying one of the particular plurality of distinct~~ the range of multiple addresses is predetermined.

20. (previously presented) The medium of claim 9, wherein the memory is a first-in-first-out memory.